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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JAIN, RAJ K	

ART UNIT	PAPER NUMBER
2416	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/619,144	CHEN, APHRODITE	
	Examiner	Art Unit	
	RAJ JAIN	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alexander (USP 6,553,029 B1) in view of Tursich (USP 6,671,828 B1).

Regarding claim(s) 1 and 9, Alexander discloses a multiple port single chip Ethernet switch (Fig. 1, with multiple incoming/outgoing ports) comprising at least the following component parts:

a physical layer entity (PHY) including a plurality of ports (Fig. 1, with multiple incoming/outgoing ports); an address table 12 for being written to and read out information to operate the plurality of ports (col 4 lines 21-26); and an address resolution control logic 10 including a source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip (col 4 lines 39-44, an address learning is invoked via the address resolution unit 10 to incorporate new addresses not in the table 12); wherein said component parts of said Ethernet switch are formed on said single chip (Fig. 1, has address resolution 10 and address table 12 on single chip).

Alexander fails to disclose a daisy chin test mode.

Tursich discloses a daisy chin test mode (Fig. 1, col 1 line 65- col 2 lines 5). Daisy chain test sequence allows for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers. The system is implemented with simple control processing that does not add significant cost or complexity to the packet network or to the protocol analyzers. Thus it would have been obvious at the time the invention was

made to incorporate the teachings of Tursich within Alexander so as to allow for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers.

Regarding claim(s) 2 and 10, Alexander discloses an input (Fig. 1, inputs at 10) for receiving the test packet.

Regarding claim(s) 3 and 11, Tursich discloses a packet generator (Fig. 1, test computer 140 generates test packet) for generating the test packet. Reasons for combining same as for claim 1.

Regarding claim(s) 4, Alexander discloses a register for storing information of the test packet (Fig. 1, table 12 is storage for all packets).

Regarding claim(s) 5 and 12, Alexander discloses a verification unit for verifying the test packet (Fig. 1, cpu 14 verifies packets).

Regarding claim(s) 6 and 13, Alexander discloses an output for sending out the test packet (Fig. 1, output at 16).

Regarding claim(s) 7, Alexander discloses wherein the source address learning engine includes a writing apparatus for writing a set of initial addresses to the address table under the daisy chain test mode (Fig. 1, 10 address resolution learns and writes the addresses to table 12).

Regarding claim(s) 8 and 14, Alexander discloses the packet source address learning process sets a packet destination address as a next port ((Fig. 1, 10 address resolution learns and writes the addresses of next ports to table 12).

Response to Arguments

Applicant's arguments filed 10/28/08 have been fully considered but they are not persuasive.

With respect to claim(s) 1 and 9, Applicant contends "Alexander fails to disclose a test for an Ethernet switch."

Examiner admits that Alexander fails to a daisy chain test mode and therefore have relied on Tursich which discloses a daisy chin test mode (Fig. 1, col 1 line 65- col

2 lines 5). Alexander was used to illustrate the use of a multiple port single chip Ethernet switch (Fig. 1, with multiple incoming/outgoing ports).

Applicant further contends "Alexander fails to disclose that the learning function performs a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip. In other words, although Alexander mentions an "address resolution unit", Alexander fails to disclose "a source address learning engine for performing a packet source address learning process under the daisy chain test mode"".

First off, Examiner fails to understand Applicants contention, Applicant has merely recited elements of either the claim and/or the cited portions of supplied references without providing a clear explanation of how the missing limitations are not met. With that said, Examiner respectfully disagrees, Alexander discloses an address resolution unit (Fig. 1, ref 10) one skilled in the art will agree that a resolution protocol inherently incorporates a "learning" algorithm that is stored within a memory storage module, furthermore, Alexander is replete with learning as part of its objective (see col 1 item 3, col 4 lines 37-41, line 66- col 5 lines 1-67). While Alexander again does not illustrate a testing function within a daisy chain environment, this deficiency is satisfied by Tursich which discloses a daisy chin test mode (Fig. 1, col 1 line 65- col 2 lines 5). Daisy chain test sequence allows for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers. The system is implemented with simple control processing that does not add significant cost or complexity to the packet network or to

the protocol analyzers. Thus it would have been obvious at the time the invention was made to incorporate the teachings of Tursich within Alexander so as to allow for a cost-effective test system that controls the traffic in a daisy-chain of protocol analyzers.

Applicant further contends Tursich fails to disclose the limitations of claim 1 same as for Alexander.

Examiner respectfully asserts that the combination of references of Alexander in view of Turshich do in fact disclose all limitations of claims 1 and 9 and therefore the rejection to claims 1 and 9 is sustained.

Furthermore, the rejection to claims 2-8 and 10-14 is also sustained as properly rejected under above cited art(s).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAJ JAIN whose telephone number is (571)272-3145. The examiner can normally be reached on M-TH.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Trost can be reached on 571-272-7872. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Raj Jain/

Examiner, Art Unit 2416